88. The rejection of claims 64, 69, 85, and 88 is therefore rendered moot. Applicants reserve the right to argue the merits of claims 64, 69, 85, and 88 in future continuation applications.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections, and that they be withdrawn. The Examiner is invited to telephone the undersigned representative if an interview might be useful for any reason.

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Respectfully submitted,
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Appendix: Amended Claims in Marked-Up Form

42. (Amended) A computer system, comprising:

a bus;

a central processing unit coupled to said bus; and

a graphics accelerator coupled to said bus, said graphics accelerator including a texture cache system, said texture cache system including a texture cache memory that stores texels to be used by a texel value generating circuit, a cache controller that performs a replacement policy determination for texel data to be stored in [controls] said texture cache memory [in accordance with a replacement policy], and a direct memory access engine that retrieves texel data from memory.

43. (Amended) The computer system of claim 42, wherein said texture cache memory is fully associative.

44. (Amended) The computer system of claim 42, wherein said replacement policy determination is performed in accordance with a least recently loaded policy.

45. (Amended) The computer system of claim 42, wherein said replacement policy determination operates such that cache lines containing texels that are being used to compute texture values to describe a polygon cannot be overwritten until said polygon is complete.

46. (Amended) The computer system of claim 45, wherein said replacement policy determination is [implemented] performed using at least one set of flags that are associated with cache lines of said texture cache.

52. (Amended) A texture mapping method using a graphics accelerator, said graphics accelerator including a texture cache memory, a cache controller [that controls the texture cache memory in accordance with a cache replacement policy], and a direct memory access engine, comprising:

(a) retrieving texels from memory via the direct memory access engine;

(b) storing said retrieved texels in the texture cache memory [in accordance with] based on a replacement policy [that is determined] determination that is performed by the cache controller; and

(c) rendering a polygon using texels that are stored in the texture cache memory.

53. (Amended) The texture mapping method of claim 52, wherein said storing comprises storing said retrieved texels in a fully associative texture cache memory.

54. (Amended) The texture mapping method of claim 52, wherein said replacement policy determination is performed in accordance with a least recently loaded policy.

55. (Amended) The texture mapping method of claim 52, wherein said replacement policy determination operates such that cache lines containing texels that are being used to compute texture values to describe a polygon cannot be overwritten until said polygon is complete.

70. (Amended) A graphics processing apparatus, comprising:

a graphics accelerator, said graphics accelerator, including

a texture cache memory;

a direct memory access engine coupled to a bus, wherein texel data is retrieved, by said direct memory access engine, from a memory over said bus and provided to said texture cache memory for storage; and

a texture engine coupled to said texture cache memory; said texture engine receiving texels from said texture cache memory to produce texture values for pixels,

wherein storage in said texture cache memory is [controlled] based on a replacement policy determination that is performed by a texture cache controller resident on said graphics accelerator[, said texture cache controller controlling said texture cache memory in accordance with a texture cache replacement policy].

71. (Amended) A graphics accelerator for use in a computer system having a central processing unit, comprising:

a texture cache memory;

a direct memory access circuit that retrieves texel data from memory;

a texture value generating circuit coupled to said texture cache memory; said texture value generating circuit producing texture values for pixels based on texel data stored in said texture cache memory; and

a cache controller that [controls] performs a replacement policy determination for said texture cache memory [in accordance with a texture cache replacement policy].

72. (Amended) The graphics accelerator of claim 71, wherein said texture cache memory is fully associative.

73. (Amended) The graphics accelerator of claim 71, wherein said [texture cache] replacement policy determination is performed in accordance with a least recently loaded policy.

74. (Amended) The graphics accelerator of claim 71, wherein said [texture cache] replacement policy determination operates such that cache lines containing texels that are being used to compute texture values to describe a polygon cannot be overwritten until said polygon is complete.

75. (Amended) The graphics accelerator of claim 74, wherein said [texture cache] replacement policy determination is [implemented] performed using at least one set of flags that are associated with cache lines of said texture cache.

76. (Amended) The graphics accelerator of claim 71, wherein said direct memory access [engine] circuit implements a virtual-physical address translation.